In the Claims:

Please cancel, without prejudice, claims 15-25 and 75-77.

Please amend claim 78 as follows:

78.(Currently Amended) The method of claim 26, further comprising:

forming a photoresist over at least a portion of said anti-reflective layer;

irradiating said photoresist, wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates said photoresist by 70% or more; and

wherein said subsequently removing ~~etching~~ a portion of said exposed portion of the dielectric layer and a portion of said bottom electrode layer comprises performing an etch using said photoresist~~, thereby exposing at least a portion of said semiconductor body and forming one or more capacitors~~.

Please amend claims 81-83 as follows:

81.(Currently Amended) A method of forming an integrated circuit, comprising:

a process flow for forming one or more transistors including:

forming a conductive layer on a semiconductor body;

subsequently forming an anti-reflective layer; and

defining and etching the conductive layer using the anti-reflective layer; and

~~an optional~~ performing a capacitor process module ~~including,~~ subsequent to said forming a conductive layer and prior to said forming an anti-reflective layer, comprising:

forming a top capacitor electrode over a portion of said conductive layer; and

forming a capacitor dielectric ~~layer~~ between said top electrode and said conductive layer, wherein said defining and etching the conductive layer forms the gate of one or more transistors and a bottom capacitor electrode,

wherein the process parameters of the portions of said process flow for forming one or more transistors prior to and subsequent to said performing a capacitor process module are optimized with ~~for the case when~~ the ~~optional~~ capacitor process module ~~is~~

omitted, and wherein the process parameters for the ~~optional~~ capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with ~~for the case when~~ the capacitor process module ~~is~~ omitted.

82.(Currently Amended) The method of claim 81, wherein said forming a top capacitor electrode and said forming a capacitor dielectric ~~optional capacitor process module~~ comprises:

forming a dielectric layer over at least a portion said conductive layer;

forming a top electrode layer over at least a portion of said conductive layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming said top capacitor electrode; and

removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said conductive layer, thereby forming said capacitor dielectric ~~layer~~ between said top electrode and said conductive layer; and

wherein said capacitor process module further comprises:

~~subsequently~~ forming a conformal insulating layer over the structure resultant from said removing at least a portion of said exposed portion of the dielectric layer ~~at least a portion of said exposed portion of the conductive layer proximate to said exposed capacitor dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer~~.

83.(Currently Amended) The method of claim 82, wherein the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with ~~for the case when~~ the capacitor process module ~~is~~ omitted.

Please amend claim 85 as follows:

85.(Currently Amended) The method of claim 81, wherein said defining and etching the conductive layer using the anti-reflective layer comprises:

forming the anti-reflective layer over the conductive layer ~~and, when the optional capacitor process module is included~~, the top capacitor electrode and the dielectric layer between said top electrode and said conductive layer;

forming a patterned mask over the anti-reflective layer; and

~~and~~ etching said conductive layer using said patterned mask.

Please add the following new claims:

86.(New) A method, comprising:

a) defining a CMOS process flow, comprising:

i) optimizing parameter values of a transistor flow to form a conductive layer, thereafter to form an anti-reflective layer on the conductive layer, and thereafter to define and etch the conductive layer using the anti-reflective layer, whereby the control gates of one or more transistor gates are formed, and wherein said etch is performed using a photoresist and said parameter values of the transistor flow include the thickness of the photoresist; and

ii) subsequently defining parameter values for a capacitor module to form a capacitor structure comprising a top electrode over a portion of said conductive layer and a capacitor dielectric therebetween and thereafter to form an insulating structure, wherein said defining and etching the conductive layer using the anti-reflective layer additionally forms a bottom electrode for said capacitor structure, and wherein the parameter values for the insulating structure of the capacitor module are optimized to electrically isolate the top electrode from the bottom electrode without changing the previously optimized parameter values of said transistor flow; and

b) forming an integrated circuit including one or more capacitors according to said CMOS process flow.

87.(New) The method of claim 86, wherein said insulating structure includes:

a conformal dielectric layer formed over said capacitor structure, wherein said parameter values for the insulating structure of the capacitor module includes a thickness for said conformal dielectric layer.

88.(New) The method of claim 86, wherein said CMOS process flow is for a process on a scale of 0.35μm or less

89.(New) The method of claim 86, wherein the said parameter values of the transistor flow further include thickness of said antireflective layer.

90.(New) The method of claim 86, wherein said capacitors have a leakage current of not greater than 4fA/μm^2.

91.(New) A method of forming an integrated circuit, comprising, in a first sector and a second sector, a process of:

a) forming a conductive layer on a semiconductor body;

b) forming an anti-reflective layer over the conductive layer;

c) forming a patterned mask over the anti-reflective layer; and

d) etching the conductive layer using the patterned mask, thereby forming the gate of one or more transistors in the first sector, wherein a), b), c) and d) are performed according to a first set of process parameters including the thickness of said mask that have been optimized for said gate formation; and

the method further comprising, in said second sector, performing a process prior to said forming an anti-reflective layer comprising:

e) forming a capacitor structure including a top electrode over a portion of said conductive layer and a capacitor dielectric therebetween, wherein said etching additionally forms a bottom capacitor electrode in the second sector; and

f) forming an insulating structure over the capacitor structure, wherein said forming an insulating structure is performed according to a second set of process parameters optimized to electrically isolate said top electrode from the conductive layer while keeping said first set of process parameters the same.

92.(New) The method of claim 91, wherein said forming an insulating structure comprises:

forming a conformal dielectric layer over said capacitor structure and said conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

93.(New) The method of claim 91, wherein the method is for a CMOS fabrication process.

94.(New) The method of claim 93, wherein the method is for a CMOS processes on a scale of 0.35μm or less.

95.(New) The method of claim 91, wherein the first set of process parameters further includes the thickness of said antireflective layer.

96.(New) The method of claim 91, wherein the method forms a capacitor structure having leakage current between the top electrode from the conductive layer of not greater than 4fA/μm^2.

97.(New) A CMOS fabrication method, comprising:

a) performing a first fabrication process, comprising:

forming a first conducting layer on a first semiconductor body;

forming a first antireflective layer over the first conductive layer;

forming a first patterned photoresist layer over the first antireflective layer; and

etching the first conductive layer using said first patterned photoresist layer into gates for one or more transistors, wherein said forming a conducting layer, forming an antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the first fabrication process on the first semiconductor body are defined by a first set of process parameters including the thickness of the photoresist that are optimized for said gate formation; and

b) performing a second fabrication process, comprising:

forming a second conducting layer on a second semiconductor body;

forming a capacitor structure including a top electrode over a portion of the second conductive layer and an inter-electrode therebetween;

forming a second antireflective layer over the second conductive layer and the capacitor structure;

forming a second patterned photoresist layer over the second antireflective layer;

etching the second conductive layer using the second patterned photoresist layer, thereby forming a lower capacitor electrode for the capacitor structure, wherein said forming a conducting layer, forming a antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the second fabrication process on the second semiconductor body are defined by said first set of process parameters; and

forming, subsequent to said forming a capacitor structure and prior to said forming a second antireflective layer, an insulating structure defined by a second set of process parameters optimized for electrically isolating the top electrode from the second conductive layer while keeping first set of process parameters the same.

98.(New) The method of claim 97, wherein said forming an insulating structure comprises:

forming a conformal dielectric layer formed over said capacitor structure and said second conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

99.(New) The method of claim 97, wherein said first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less.

100.(New) The method of claim 97, wherein the first set of process parameters further includes the thickness of the antireflective layer.

101.(New) The method of claim 97, wherein the second fabrication process forms a capacitor structure having leakage current between the top electrode from the second conductive layer of not greater than $4fA/\mu m^2$.